ABSTRACT OF THE DISCLOSURE

In a memory cell (110) having multiple floating gates (160), the select gate (140) is formed before the floating gates. In some embodiments, the memory cell also has control gates (170) formed after the select gate. Substrate isolation regions (220) are formed in a semiconductor substrate (120). The substrate isolation regions protrude above the substrate. Then select gate lines (140) are formed. Then a floating gate layer (160) is deposited. The floating gate layer is etched until the substrate isolation regions are exposed. A dielectric (164) is formed over the floating gate layer, and a control gate layer (170) is deposited. The control gate layer protrudes upward over each select gate line. These the control gates and the floating gates are defined independently of photolithographic alignment. In another aspect, a nonvolatile memory cell has at least two conductive floating gates (160). A dielectric layer (164) overlying the floating gate has a continuous feature that overlies the floating gate and also overlays a sidewall of the select gate (140). Each control gate (160) overlies the continuous feature of the dielectric layer and also overlies the floating gate. In another aspect, substrate isolation regions (220) are formed in a semiconductor substrate. Select gate lines cross over the substrate isolation regions. Each select gate line has a planar top surface, but its bottom surface goes up and down over the substrate isolation regions. Other features are also provided.